07 MAY 1997 15:24:04 U.S. Patent & Trademark Office P0001

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                                 *
*           Welcome to MESSENGER (APS Text) at USPTO              *
*                                                                 *
*                                                                 *
*    The USPTO production files are current through:              *
*    06 May 1997 for U.S. Patent Text Data.                      *
*    06 May 1997 for U.S. Current Classification data.           *
*    06 May 1997 for U.S. Patent Image Data.                     *
*                                                                 *
*       * PLEASE USE 305-9000 FOR NEW TELEPHONE NUMBER *          *
-*****************************************************************
*    A new set of Messenger enhancements is available,            *
*    effective December 9, 1996.  The new FOCUS command           *
*    allows you to display your search results in relevance-      *
*    ranked order.  Enter FOCUS and the L-number you want         *
*    to view (e.g., FOCUS L5), and then display the resulting     *
*    L-number (e.g., D L6 1-12).                                  *
*    See also HELP FOCUS.                                         *
*****************************************************************
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*  DISCLAIMER:                                                    *
*  Neither the United States Government, nor any agency           *
*  thereof, nor any of their contractors, subcontractors or       *
*  employees make any warranty, expressed or implied,             *
*  including any warranty of marketability of fitness for a       *
*  particular purpose; nor assumes any legal liability or         *
*  responsibility for any party's use, or the results of          *
*  such, of the data.                                             *07 MAY 1997 1
5:24:05          U.S. Patent & Trademark Office          P0002
*                                                                 *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                Help Desk --> 703-305-9000                       *
*                                                                 *
*    The Help Desk is staffed for APS support 7 days/week.        *
*      Monday through Friday:      6:30am - 9:00pm                *
*      Saturday, Sunday, Holidays: 8:30am - 5:00 pm               *
*                                                                 *
*    The Help Desk staff at this number will handle all APS       *
*    related questions.                                           *
*                                                                 *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                                 *
*    >>>>>>>>>>>> NEW SUNDAY HOURS !!! <<<<<<<<<<<<<              *
*                                                                 *
*    The APS is available:                                        *
*            6:30am - 9:00pm Monday through Friday                *
*            7:30am - 5:00pm Saturday, Sunday, Holidays           *
*                                                                 *
*      APS is unavailable Thanksgiving Day, Christmas Day,        *
*      and New Year's Day.                                        *
*                                                                 *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
FILE 'USPAT' ENTERED AT 15:24:05 ON 07 MAY 1997

* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*              W E L C O M E   T O   T H E                        *
*        U. S.   P A T E N T   T E X T   F I L E                  *
```

* *
07 MAY 1997 15:24:06 U.S. Patent & Trademark Office P0003

```
=> S BIDIRECTION## OR BI(2A)DIRECTION##
            21944 BIDIRECTION##
            47633 BI
           103822 BIS
           147356 BI
                  (BI OR BIS)
          1022702 DIRECTION##
            12438 BI(2A)DIRECTION##
L1          31815 BIDIRECTION## OR BI(2A)DIRECTION##

=> S (FIRST(2A)L1) AND (SECOND(2A)L1)
           1550612 FIRST
               243 FIRSTS
          1550620 FIRST
                  (FIRST OR FIRSTS)
               835 FIRST(2A)L1
           1417073 SECOND
            192657 SECONDS
          1462827 SECOND
                  (SECOND OR SECONDS)
               852 SECOND(2A)L1
L2             509 (FIRST(2A)L1) AND (SECOND(2A)L1)

=> S L2 AND INTERFAC##
           192105 INTERFAC##
L3             189 L2 AND INTERFAC##

=> S L2(P)INTERFACE#
*WARNING* - PROXIMITY OPERATOR PRECEDENCE LEVEL CONFLICTS OR IS NOT CONSISTENT
WITH
FIELD CODE - 'AND' OPERATOR ASSUMED 'L2(P)INTERFACE#'
           192081 INTERFACE#
L4             189 L2(P)INTERFACE#

=> S L3 AND BUS
            78683 BUS
            20619 BUSES
             7109 BUSSES
            84116 BUS
                  (BUS OR BUSES OR BUSSES)
L5             134 L3 AND BUS

=> S L5 AND PRINTER#
            63205 PRINTER#
L6              20 L5 AND PRINTER#

=> D L6 1-20
```

1. 5,590,374, Dec. 31, 1996, Method and apparatus for employing a dummy read command to automatically assign a unique memory address to an **interface** card; Ryan E. Shariff, et al., 395/829, 284, 830 [IMAGE AVAILABLE]

2. 5,582,593, Dec. 10, 1996, Ambulatory medication delivery system; Barry W. Hultman, 604/65 [IMAGE AVAILABLE]

3. 5,519,410, May 21, 1996, Virtual image display management system with head-up display; Joseph P. Smalanskas, et al., 345/7; 340/980 [IMAGE AVAILABLE]

4. 5,485,627, Jan. 16, 1996, Partitionable massively parallel processing system; W. Daniel Hillis, 395/800; 364/228.7, 228.9, 229, 229.1, 229.4, 229.5, DIG.1; 395/311 [IMAGE AVAILABLE]

5. 5,420,696, May 30, 1995, Image data transfer architecture and method for an electronic reprographic machine; Donald L. Wegeng, et al., 358/468; 345/190; 358/406; 395/526 [IMAGE AVAILABLE]

6. 5,175,865, Dec. 29, 1992, Partitioning the processors of a massively parallel single array processor into sub-arrays selectively controlled by host computers; W. Daniel Hillis, 395/800; 364/228.7, 228.9, 229, 229.1, 229.2, 229.4, 229.5, 231, 231.9, 240, 240.1, 240.2, 247, 247.8, 249, 249.2, 265, 265.3, 266.3, 266.5, 271, 271.2, 271.4, 274, 274.1, 275, DIG.1; 395/309 [IMAGE AVAILABLE]

7. 4,914,619, Apr. 3, 1990, Apparatus and method for interconnecting an application of a transparent services access facility to remote source; John F. Harris, et al., 395/200.09; 364/228.2, 232.1, 926.1, 926.93, 927.92, 927.96, 929, 930, 931, 931.4, 931.43, 933.9, 935, 935.2, 935.3, 935.4, 940, 940.61, 940.64, 940.81, 941, 943.9, 946.2, 947, 950.1, 964.1, 976, 978.1, DIG.2 [IMAGE AVAILABLE]

8. 4,839,830, Jun. 13, 1989, Apparatus and method for the processing of operating data of an electric motor; Walter Amey, et al., 364/551.01, 508 [IMAGE AVAILABLE]

9. 4,833,655, May 23, 1989, FIFO memory with decreased fall-through delay; Michael A. Wolf, et al., 365/221, 73, 230.05; 371/51.1; 377/67 [IMAGE AVAILABLE]

10. 4,548,134, Oct. 22, 1985, Dot image buffer and dot sequence scrambler for dot matrix line **printer**; Donald K. Wadley, et al., 101/93.04, 93.05; 346/78 [IMAGE AVAILABLE]

11. 4,547,845, Oct. 15, 1985, Split-**BUS** multiprocessor system; Jerry H. Ross, 395/289; 364/229.4, 238, 238.5, 239, 239.6, 240.1, 241, 241.2, 242, 242.4, 242.5, 243, 243.7, 259, 260.4, 260.8, 260.9, 270.5, 270.6, DIG.1 [IMAGE AVAILABLE]

12. 4,525,780, Jun. 25, 1985, Data processing system having a memory using object-based information and a protection scheme for determining access rights to such information; Richard G. Bratt, et al., 395/490; 364/228.3, 231.4, 231.6, 243, 244, 244.3, 246.6, 262.4, 262.8, 263, 286, 286.4, 286.5, DIG.1 [IMAGE AVAILABLE]

13. 4,493,027, Jan. 8, 1985, Method of performing a call operation in a digital data processing system having microcode call and return operations; Lawrence H. Katz, et al., 395/569; 364/228.2, 228.5, 241.2, 244, 244.3, 247, 247.7, 256.3, 258, 260, 260.1, 261.3, 262.4, 262.7, 262.8, 270.5, 280.4, DIG.1; 395/590, 595 [IMAGE AVAILABLE]

14. 4,470,113, Sep. 4, 1984, Information processing unit; Toshio Oura, 395/306; 364/221, 221.6, 228.4, 228.6, 229, 229.2, 230, 230.4, 232.7, 232.8, 232.9, 238.3, 240, 240.1, 240.2, 240.4, 240.5, 241.9, 242.1, 260, 260.1, 275.7, 275.9, 284, DIG.1 [IMAGE AVAILABLE]

15. 4,455,602, Jun. 19, 1984, Digital data processing system having an I/O means using unique address providing and access priority control techniques; Ward Baxter, III, et al., 395/825; 364/228.1, 228.3, 231.4, 231.6, 232.1, 243, 243.3, 244, 244.3, 246.6, 262.4, 262.8, 263, 280, 280.4, 281.3, 281.4, DIG.1; 395/859, 885 [IMAGE AVAILABLE]

16. 4,445,177, Apr. 24, 1984, Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions; Richard G. Bratt, et al., 395/800; 364/228.3, 231.4, 231.6, 232.1, 238.4, 239, 239.7, 241.2, 241.3, 241.5, 241.9, 243, 243.4, 243.41, 243.43, 244, 244.3, 244.6, 246.6, 246.7, 246.8, 246.9, 246.91, 247, 247.2, 247.7, 247.8, 254, 254.3, 254.5, 256.8, 258, 258.2, 258.3, 259, 259.5, 259.8, 261.3, 261.6, 262.4, 262.7, 262.8, 262.81, 263, 263.2, 263.3, 265, 265.3, 266, 266.1, 267, 267.6, 267.9, 270, 270.1, 271, 271.3, 271.4, 271.6, 271.8, 280, 280.1, 280.4, 280.8, 280.9, 281, 281.3, 281.4, 281.5, 281.6, 281.7, 281.8, 282, 282.1, 282.2, 284, 284.3, DIG.1 [IMAGE AVAILABLE]

17. 4,388,686, Jun. 14, 1983, Communication system for distributed control arrangement; William R. Haid, 395/308; 364/222.2, 222.3, 226.8, 226.9, 228.3, 229, 229.2, 232.7, 232.8, 234, 235, 237.2, 237.3, 238.3, 238.4, 238.5, 239, 239.4, 240, 240.1, 243, 243.3, 244, 244.6, 244.7, 249, 249.2, 251, 251.1, 251.3, 252, 252.3, 252.6, 259, 259.1, 259.2, 259.4, 260.4, 260.5, 264, 264.5, 268, 268.3, 268.7, 270, 270.1, 270.5, 270.7, 271, 271.2, DIG.1; 395/250 [IMAGE AVAILABLE]

18. 4,272,829, Jun. 9, 1981, Reconfigurable register and logic circuitry device for selective connection to external **buses**; Carson T. Schmidt, et al., 395/800; 327/403; 364/927.8, 932, 933, 933.3, 934, 935, 935.2, 935.3, 935.4, 935.45, 935.46, 936.1, 937.1, 940, 940.1, 940.2, 942.3, 942.4, 946.2, 946.6, 947, 947.1, 947.4, 948.1, 964, 964.2, DIG.2 [IMAGE AVAILABLE]

19. 4,234,926, Nov. 18, 1980, System & method for monitoring & diagnosing faults in environmentally controlled containers, such system and method being especially adapted for remote computer controlled monitoring of numerous transportable containers over existing on-site power wiring; Clifford G. Wallace, et al., 364/551.01, 131, 138, 185, 919, 919.5, 920, 921.8, 926, 927, 927.2, 927.4, 927.8, 927.82, 927.83, 927.92, 927.95, 927.99, 929.4, 930, 931, 931.4, 932.8, 935, 935.2, 935.3, 937, 939, 939.5, 940, 940.1, 940.2, 942, 943.9, 944.91, 947, 947.2, 949, 949.5, 952, 952.1, 959.1, 964, 964.1, 965, 965.5, 965.76, DIG.2 [IMAGE AVAILABLE]

20. 4,232,199, Nov. 4, 1980, Special services add-on for dial pulse activated telephone switching office; John T. Boatwright, et al., 379/197, 201, 205, 243, 246 [IMAGE AVAILABLE]

```
=> D HIS

     (FILE 'USPAT' ENTERED AT 15:24:05 ON 07 MAY 1997)

                SET PAGE SCROLL
L1         31815 S BIDIRECTION## OR BI(2A)DIRECTION##
L2           509 S (FIRST(2A)L1) AND (SECOND(2A)L1)
L3           189 S L2 AND INTERFAC##
L4           189 S L2(P)INTERFACE#
L5           134 S L3 AND BUS
L6            20 S L5 AND PRINTER#

=> S L6 AND CONTROL##
              998125 CONTROL##
L7            20 L6 AND CONTROL##
```

```
=> S L5 AND (PRINT### OR DISPLAY### OR READ###)
            217216 PRINT###
            245432 DISPLAY###
           1041680 READ###
   L8          130 L5 AND (PRINT### OR DISPLAY### OR READ###)

=> S L8 AND CONTROL####
                  1182307 CONTROL####
L9          130 L8 AND CONTROL####

=> S L9 AND (PC OR COMPUTER)
            26610 PC
             2197 PCS
            27806 PC
                    (PC OR PCS)
           176338 COMPUTER
            43173 COMPUTERS
           187517 COMPUTER
                    (COMPUTER OR COMPUTERS)
L10          94 L9 AND (PC OR COMPUTER)

=> D L10 1-94
```

1. 5,627,976, May 6, 1997, Crossing transfers for maximizing the effective bandwidth in a dual-**bus** architecture; Harold L. McFarland, et al., 395/308, 306 [IMAGE AVAILABLE]

2. 5,619,642, Apr. 8, 1997, Fault tolerant memory system which utilizes data from a shadow memory device upon the detection of erroneous data in a main memory device; Michael E. Nielson, et al., 395/182.04, 183.18, 185.05, 185.07 [IMAGE AVAILABLE]

3. 5,616,269, Apr. 1, 1997, **Control** system for a microwave oven and method of making the same; Daniel L. Fowler, et al., 219/720, 492, 506, 702 [IMAGE AVAILABLE]

4. 5,606,359, Feb. 25, 1997, Video on demand system with multiple data sources configured to provide vcr-like services; John J. Youden, et al., 348/7, 12, 13; 455/5.1 [IMAGE AVAILABLE]

5. 5,598,550, Jan. 28, 1997, Cache **controller** for processing simultaneous cache accesses; Gene W. Shen, et al., 395/473, 427, 458, 478 [IMAGE AVAILABLE]

6. 5,598,408, Jan. 28, 1997, Scalable processor to processor and processor to I/O interconnection network and method for parallel processing arrays; John R. Nickolls, et al., 370/351, 380, 388; 395/200.01, 312, 800 [IMAGE AVAILABLE]

7. 5,592,629, Jan. 7, 1997, Apparatus and method for matching data rates to transfer data between two asynchronous devices; William H. Gamble, 395/250 [IMAGE AVAILABLE]

8. 5,592,538, Jan. 7, 1997, Telecommunication device and method for interactive voice and data; Richard P. Kosowsky, et al., 379/93, 88, 96, 97, 98, 355 [IMAGE AVAILABLE]

9. 5,590,374, Dec. 31, 1996, Method and apparatus for employing a dummy **read** command to automatically assign a unique memory address to an

interface card; Ryan E. Shariff, et al., 395/829, 284, 830 [IMAGE AVAILABLE]

10. 5,582,593, Dec. 10, 1996, Ambulatory medication delivery system; Barry W. Hultman, 604/65 [IMAGE AVAILABLE]

11. 5,572,160, Nov. 5, 1996, Architecture for RF signal automatic test equipment; Brian C. Wadell, 327/427; 324/763; 333/101, 109 [IMAGE AVAILABLE]

12. 5,541,640, Jul. 30, 1996, Videophone for simultaneous audio and video communication via a standard telephone line; Craig R. Larson, 348/19; 379/96 [IMAGE AVAILABLE]

13. 5,539,448, Jul. 23, 1996, Video server that adapts video signals from memory to a format compatible with a communication system in a video-on-demand network; Henri A. J. Verhille, et al., 348/6, 7, 16 [IMAGE AVAILABLE]

14. 5,495,589, Feb. 27, 1996, Architecture for smart **control** of bi-directional transfer of data; Donald W. Mackenthun, et al., 395/200.15; 364/242.94, DIG.1; 395/800 [IMAGE AVAILABLE]

15. 5,493,534, Feb. 20, 1996, Remotely re-programmable program memory for a microcontroller; Tsung D. Mok, 365/226, 185.33, 189.01 [IMAGE AVAILABLE]

16. 5,486,824, Jan. 23, 1996, Data processor with a hardware keyscan circuit, hardware keyscan circuit, and method therefor; Keith E. Kinerk, et al., 341/26; 340/825.77; 341/24, 25; 364/189 [IMAGE AVAILABLE]

17. 5,485,627, Jan. 16, 1996, Partitionable massively parallel processing system; W. Daniel Hillis, 395/800; 364/228.7, 228.9, 229, 229.1, 229.4, 229.5, DIG.1; 395/311 [IMAGE AVAILABLE]

18. 5,481,542, Jan. 2, 1996, Interactive information services **control** system; Gary L. Logston, et al., 348/7, 13; 370/442, 461, 473, 474 [IMAGE AVAILABLE]

19. 5,473,666, Dec. 5, 1995, Method and apparatus for digitally **controlling** gain in a talking path; Edward J. Szczebak, Jr., et al., 379/3; 375/345; 379/402 [IMAGE AVAILABLE]

20. 5,471,481, Nov. 28, 1995, Testing method for electronic apparatus; Koji Okumoto, et al., 371/22.3; 324/73.1; 371/22.1, 25.1, 27 [IMAGE AVAILABLE]

21. 5,448,700, Sep. 5, 1995, Method and system for interfacing **PC** to CD-ROM drives; Dae Y. Kim, 395/310; 364/235.3, 236.1, 236.2, 243.3, DIG.1; 395/438, 848 [IMAGE AVAILABLE]

22. 5,440,108, Aug. 8, 1995, System and method for dispensing and revalung cash cards; Dich C. Tran, et al., 235/381, 380, 487, 492 [IMAGE AVAILABLE]

23. 5,434,404, Jul. 18, 1995, Linear scanner apparatus for communicating with a data card; Yiu T. Liu, et al., 235/475, 384, 476, 477 [IMAGE AVAILABLE]

24. 5,430,762, Jul. 4, 1995, Expandable repeater; Nader Vijeh, et al., 375/211; 370/445 [IMAGE AVAILABLE]

25. 5,426,738, Jun. 20, 1995, Apparatus for flexibly routing signals between pins of electronic devices; Wen-Jai Hsieh, et al., 307/112; 364/239, DIG.1; 395/250 [IMAGE AVAILABLE]

26. 5,420,696, May 30, 1995, Image data transfer architecture and method for an electronic reprographic machine; Donald L. Wegeng, et al., 358/468; 345/190; 358/406; 395/526 [IMAGE AVAILABLE]

27. 5,414,820, May 9, 1995, Crossing transfers for maximizing the effective bandwidth in a dual-**bus** architecture; Harold L. McFarland, et al., 395/308; 364/240, 240.2, 240.5, 242.6, 242.92, DIG.1; 370/438; 395/309 [IMAGE AVAILABLE]

28. 5,404,547, Apr. 4, 1995, System for storing different categories of routines in internal and external memories respectively and executing the routines based upon impact by generated noise; Menachem Diamantstein, et al., 455/73; 364/221.1, 221.9, 230.3, DIG.1; 395/181, 308, 653; 455/899 [IMAGE AVAILABLE]

29. 5,388,227, Feb. 7, 1995, Transparent data **bus** sizing; Harold L. McFarland, 395/307; 364/238.6, 239.5, 240, 240.1, 240.3, 243, 260, DIG.1 [IMAGE AVAILABLE]

30. 5,379,052, Jan. 3, 1995, VGA and EGA video **controller** apparatus using shared common video memory; Jeffrey A. Walck, et al., 345/185, 132 [IMAGE AVAILABLE]

31. 5,361,376, Nov. 1, 1994, Keyboard and **controller** with a three wire half duplex asynchronous and bidirectional communications architecture; Dennis A. Cummins, et al., 395/800; 364/228, 234, 238.3, DIG.1; 395/893 [IMAGE AVAILABLE]

32. 5,349,683, Sep. 20, 1994, Bidirectional FIFO with parity generator/checker; Sheau-Dong Wu, et al., 395/800; 364/244.3, 965.4, DIG.1, DIG.2 [IMAGE AVAILABLE]

33. 5,298,672, Mar. 29, 1994, Electronic musical instrument with memory **read** sequence **control**; Rainer Gallitzendorfer, 84/603, 604, 607, 622; 364/723 [IMAGE AVAILABLE]

34. 5,280,590, Jan. 18, 1994, Logic support chip for AT-type **computer** with improved **bus** architecture; R
obert M. Pleva, et al., 395/309; 364/231,
232.8, 239, 246, 246.11, DIG.1; 395/250 [IMAGE AVAILABLE]

35. 5,280,474, Jan. 18, 1994, Scalable processor to processor and processor-to-I/O interconnection network and method for parallel processing arrays; John R. Nickolls, et al., 370/389; 371/49.3 [IMAGE AVAILABLE]

36. 5,265,123, Nov. 23, 1993, Expandable repeater; Nader Vijeh, et al., 375/211, 213 [IMAGE AVAILABLE]

37. 5,262,771, Nov. 16, 1993, Method for addressing processor units; Karl Herrmann, et al., 340/825.08, 825.03, 825.07, 825.5 [IMAGE AVAILABLE]

38. 5,247,643, Sep. 21, 1993, Memory **control** circuit for optimizing copy back/line fill operation in a copy back cache system; Shmuel Shottan, 395/470; 364/DIG.1 [IMAGE AVAILABLE]

39. 5,233,616, Aug. 3, 1993, Write-back cache with ECC protection; Michael A. Callander, 371/37.7, 40.2 [IMAGE AVAILABLE]

40. 5,226,124, Jul. 6, 1993, Communication **interface** between a radio

control transmitter and a **computer** data **bus**; David R. Stern, 395/892; 340/825.69; 341/176; 364/926.1, 926.3, 927.92, 927.93, 927.94, 927.95, 932.8, 939, 947, 947.1, DIG.2; 395/250 [IMAGE AVAILABLE]

41. 5,225,974, Jul. 6, 1993, Programmable **controller** processor with an intelligent functional module **interface**; Kathleen B. Mathews, et al., 364/140, 136, 926.9, 947.4, 949, DIG.2; 395/821 [IMAGE AVAILABLE]

42. 5,175,865, Dec. 29, 1992, Partitioning the processors of a massively parallel single array processor into sub-arrays selectively **controlled** by host **computers**; W. Daniel Hillis , 395/800; 364/228.7, 228.9, 229, 229.1, 229.2, 229.4, 229.5, 231, 231.9, 240, 240.1, 240.2, 247, 247.8, 249, 249.2, 265, 265.3, 266.3, 266.5, 271, 271.2, 271.4, 274, 274.1, 275, DIG.1; 395/309 [IMAGE AVAILABLE]

43. 5,170,482, Dec. 8, 1992, Improved hypercube topology for multiprocessor **computer** systems; Renben Shu, et al., 395/800; 364/229, 229.5, 927.81, 927.92, 927.95, 931, 931.4, 931.41, 931.46, 935, 935.2, 937.1, 937.8, 940, 940.61, 940.63, 940.64, 940.67, 940.92, 942, 943.9, 944.61, 950, 950.4, 966.1, 966.4, DIG.1, DIG.2 [IMAGE AVAILABLE]

44. 5,144,314, Sep. 1, 1992, Programmable object identification transponder system; Eric Malmberg, et al., 342/44, 51 [IMAGE AVAILABLE]

45. 5,128,996, Jul. 7, 1992, Multichannel data encryption device; Michael J. Rosenow, et al., 380/21; 235/380; 380/25, 49 [IMAGE AVAILABLE]

46. 5,125,080, Jun. 23, 1992, Logic support chip for AT-type **computer** with improved **bus** architecture; R obert M. Pleva, et al., 395/309; 364/239, 246, 246.11; 395/250 [IMAGE AVAILABLE]

47. 5,056,041, Oct. 8, 1991, Data processing apparatus with improved bit masking capability; Karl M. Guttag, et al., 395/521; 345/191; 395/513 [IMAGE AVAILABLE]

48. 5,047,926, Sep. 10, 1991, Development and debug tool for microcomputers; Ruey-Shen Kuo, et al., 395/183.05; 364/237.2, 238, 239, 240, 240.2, 241.9, 244, 244.6, 252, 264, 264.6, 265, 265.5, 266.5, 267.91; 395/250 [IMAGE AVAILABLE]

49. 5,041,969, Aug. 20, 1991, Microprocessor and data processor using the former; Shumpei Kawasaki, et al., 395/581; 364/222.8, 228, 230, 230.3, 230.4, 232.8, 238, 240.1, 244, 244.9, 247, 247.1, 247.7, 247.8, 251, 251.3, 258, 259.9, 260, 261.3, 261.4, 261.5, 262.4, 264, 264.6, 281.3, 281.4, DIG.1 [IMAGE AVAILABLE]

50. 4,980,845, Dec. 25, 1990, Digital engine analyzer; Michael C. Putrow, et al., 364/550, 424.038, 431.04, 431.12 [IMAGE AVAILABLE]

51. 4,964,046, Oct. 16, 1990, Harvard architecture microprocessor with arithmetic operations and **control** tasks for data transfer handled simultaneously; Soenke Mehrgardt, et al., 395/250; 364/239, 239.1, 240, 240.2, 270, DIG.1; 395/590 [IMAGE AVAILABLE]

52. 4,908,823, Mar. 13, 1990, Hybrid communications link adapter incorporating input/output and data communications technology; Randolph B. Haagens, et al., 370/464; 340/825.03, 825.2, 825.5; 359/158, 163; 370/466; 375/222 [IMAGE AVAILABLE]

53. 4,891,751, Jan. 2, 1990, Massively parallel vector processing **computer**; Duane B. Call, et al., 395/800; 364/231.9, 232.21, 236.2, 238, 240, 240.1, 242.3, 242.31, 242.94, DIG.1 [IMAGE AVAILABLE]

54. 4,833,655, May 23, 1989, FIFO memory with decreased fall-through delay; Michael A. Wolf, et al., 365/221, 73, 230.05; 371/51.1; 377/67 [IMAGE AVAILABLE]

55. 4,804,938, Feb. 14, 1989, Distribution energy management system; Donald W. Rouse, et al., 340/310.06, 310.02, 310.07, 825.06; 375/206, 259; 455/3.3, 5.1 [IMAGE AVAILABLE]

56. 4,787,082, Nov. 22, 1988, Data flow **control** arrangement for local area network; Robert H. Delaney, et al., 370/216, 235, 397, 402, 407, 447, 449 [IMAGE AVAILABLE]

57. 4,768,188, Aug. 30, 1988, Optical demand assigned local loop communication system; Andrew W. Barnhart, et al., 370/434, 442, 510, 516, 535 [IMAGE AVAILABLE]

58. 4,760,518, Jul. 26, 1988, Bi-directional databus system for supporting superposition of vector and scalar operations in a **computer**; Hanan Potash, et al., 395/287; 364/730, DIG.1 [IMAGE AVAILABLE]

59. 4,744,281, May 17, 1988, Automatic sound player system having acoustic and electronic sound sources; Yoshimasa Isozaki, 84/602, 171, 645, DIG.4; 984/71, 212, DIG.1 [IMAGE AVAILABLE]

60. 4,742,343, May 3, 1988, Digital stroke generator; Ciaran O'Donnell, 345/16 [IMAGE AVAILABLE]

61. 4,727,509, Feb. 23, 1988, Master/slave system for replicating/formatting flexible magnetic diskettes; Ronald R. Johnson, et al., 360/15, 73.03; 364/DIG.2 [IMAGE AVAILABLE]

62. 4,665,479, May 12, 1987, Vector data processing system for indirect address instructions; Yuji Oinaga, 395/800; 364/232.21, 242.6, 242.7, 244, 244.8, 247, 264, 264.6, 736, DIG.1 [IMAGE AVAILABLE]

63. 4,652,933, Mar. 24, 1987, Image information processing system; Takaho Koshiishi, 358/426, 434, 442, 469; 379/100 [IMAGE AVAILABLE]

64. 4,622,632, Nov. 11, 1986, Data processing system having a pyramidal array of processors; Steven L. Tanimoto, et al., 395/800; 364/222.2, 228.3, 231.9, 232.8, 232.91, 238, 243, 260, 260.1, 260.4, DIG.1 [IMAGE AVAILABLE]

65. 4,589,106, May 13, 1986, Data line card **printed** board assembly; Donald W. Prather, et al., 370/359, 369 [IMAGE AVAILABLE]

66. 4,584,680, Apr. 22, 1986, Use of a tone **bus** to provide polling and data distribution apparatus for communication system terminal groups; Nicholas J. R. Carter, et al., 370/360, 449 [IMAGE AVAILABLE]

67. 4,569,040, Feb. 4, 1986, Electronic switching system having a time division multiplex switch **controller** address by central **control** unit; Anthony J. P. O'Toole, et al., 370/364 [IMAGE AVAILABLE]

68. 4,548,134, Oct. 22, 1985, Dot image buffer and dot sequence scrambler for dot matrix line **printer**; Donald K. Wadley, et al., 101/93.04, 93.05;

346/78 [IMAGE AVAILABLE]

69. 4,547,845, Oct. 15, 1985, Split-**BUS** multiprocessor system; Jerry H. Ross, 395/289; 364/229.4, 238, 238.5, 239, 239.6, 240.1, 241, 241.2, 242, 242.4, 242.5, 243, 243.7, 259, 260.4, 260.8, 260.9, 270.5, 270.6, DIG.1 [IMAGE AVAILABLE]

70. 4,543,646, Sep. 24, 1985, Chip topography for MOS Data Encryption Standard circuit; William H. Ambrosius, III, et al., 380/29; 364/918, 918.7, 925.5, 927.8, 927.92, 927.99, 929.1, 933, 933.3, 933.7, 935.2, 935.4, 935.44, 935.45, 935.46, 943.9, 945.6, 949, 949.71, DIG.2; 380/49 [IMAGE AVAILABLE]

71. 4,528,626, Jul. 9, 1985, Microcomputer system with **bus control** means for peripheral processing devices; Mark E. Dean, et al., 395/848; 364/232.8, 240, 240.4, 242.3, 242.31, 242.32, 242.5, 244, 244.6, 252, DIG.1 [IMAGE AVAILABLE]

72. 4,525,780, Jun. 25, 1985, Data processing system having a memory using object-based information and a protection scheme for determining access rights to such information; Richard G. Bratt, et al., 395/490; 364/228.3, 231.4, 231.6, 243, 244, 244.3, 246.6, 262.4, 262.8, 263, 286, 286.4, 286.5, DIG.1 [IMAGE AVAILABLE]

73. 4,497,033, Jan. 29, 1985, Multiplexed arrangement for connecting a plurality of transducers to a field **interface** device at a storage tank; Rafael Hernandez, et al., 364/551.01; 73/304C; 340/620; 364/221, 221.7, 237.8, 238, 240.1, 264, 264.1, 509, 917, 917.5, 917.8, 920, 921.8, 921.9, 926, 926.9, 935, 935.3, 935.4, 935.5, 942, 942.06, 947, 947.2, DIG.1, DIG.2 [IMAGE AVAILABLE]

74. 4,493,027, Jan. 8, 1985, Method of performing a call operation in a digital data processing system having microcode call and return operations; Lawrence H. Katz, et al., 395/569; 364/228.2, 228.5, 241.2, 244, 244.3, 247, 247.7, 256.3, 258, 260, 260.1, 261.3, 262.4, 262.7, 262.8, 270.5, 280.4, DIG.1; 395/590, 595 [IMAGE AVAILABLE]

75. 4,485,402, Nov. 27, 1984, Video image processing system; Anthony D. Searby, 348/715 [IMAGE AVAILABLE]

76. 4,455,602, Jun. 19, 1984, Digital data processing system having an I/O means using unique address providing and access priority **control** techniques; Ward Baxter, III, et al., 395/825; 364/228.1, 228.3, 231.4, 231.6, 232.1, 243, 243.3, 244, 244.3, 246.6, 262.4, 262.8, 263, 280, 280.4, 281.3, 281.4, DIG.1; 395/859, 885 [IMAGE AVAILABLE]

77. 4,445,177, Apr. 24, 1984, Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions; Richard G. Bratt, et al., 395/800; 364/228.3, 231.4, 231.6, 232.1, 238.4, 239, 239.7, 241.2, 241.3, 241.5, 241.9, 243, 243.4, 243.41, 243.43, 244, 244.3, 244.6, 246.6, 246.7, 246.8, 246.9, 246.91, 247, 247.2, 247.7, 247.8, 254, 254.3, 254.5, 256.8, 258, 258.2, 258.3, 259, 259.5, 259.8, 261.3, 261.6, 262.4, 262.7, 262.8, 262.81, 263, 263.2, 263.3, 265, 265.3, 266, 266.1, 267, 267.6, 267.9, 270, 270.1, 271, 271.3, 271.4, 271.6, 271.8, 280, 280.1, 280.4, 280.8, 280.9, 281, 281.3, 281.4, 281.5, 281.6, 281.7, 281.8, 282, 282.1, 282.2, 284, 284.3, DIG.1 [IMAGE AVAILABLE]

78. 4,423,480, Dec. 27, 1983, Buffered peripheral system with priority queue and preparation for signal transfer in overlapped operations; Wayne J. Bauer, et al., 395/280; 364/DIG.1 [IMAGE AVAILABLE]

79. 4,420,810, Dec. 13, 1983, Apparatus for operating a motor driven device and testing state of series limit switch over same two-wire circuit; Rafael Hernandez, et al., 364/509; 340/618; 364/481 [IMAGE AVAILABLE]

80. 4,406,004, Sep. 20, 1983, Ring scheduling apparatus for a digital multiplexed telecommunication system; Jay D. Hall, et al., 370/249, 522; 379/180, 253 [IMAGE AVAILABLE]

81. 4,398,248, Aug. 9, 1983, Adaptive WSI/MNOS solid state memory system; Yukun Hsia, et al., 365/230.03; 364/231.9, 232.7, 232.8, 238.3, 238.4, 240, 240.1, 244, 244.1, 244.3, 245, 245.2, 245.3, 249, 249.2, 249.3, 251, 253, 254, 254.3, 254.4, 254.5, 256.3, 256.4, 264, 264.1, 267, 267.7, 268, 268.3, 268.5, 268.9, 269.2, 271, 273, 273.1, 273.2, 281.9, 285, 285.3, DIG.1; 365/200 [IMAGE AVAILABLE]

82. 4,388,686, Jun. 14, 1983, Communication system for distributed **control** arrangement; William R. Haid, 395/308; 364/222.2, 222.3, 226.8, 226.9, 228.3, 229, 229.2, 232.7, 232.8, 234, 235, 237.2, 237.3, 238.3, 238.4, 238.5, 239, 239.4, 240, 240.1, 243, 243.3, 244, 244.6, 244.7, 249, 249.2, 251, 251.1, 251.3, 252, 252.3, 252.6, 259, 259.1, 259.2, 259.4, 260.4, 260.5, 264, 264.5, 268, 268.3, 268.7, 270, 270.1, 270.5, 270.7, 271, 271.2, DIG.1; 395/250 [IMAGE AVAILABLE]

83. 4,387,434, Jun. 7, 1983, Intelligent field **interface** device for fluid storage facility; Marion L. Moncrief, Jr., et al., 364/509; 137/392; 340/870.16 [IMAGE AVAILABLE]

84. 4,325,121, Apr. 13, 1982, Two-level **control** store for microprogrammed data processor; Thomas G. Gunter, et al., 395/597; 364/230, 230.4, 231.8, 232.8, 232.9, 232.91, 238, 240, 240.1, 241.2, 241.3, 243, 243.3, 243.7, 244, 244.6, 252.3, 252.6, 254.9, 255, 255.1, 255.8, 259, 259.9, 260, 260.2, 261.3, 261.5, 262.4, 262.7, 262.8, 263, 263.1, 264, 264.1, 265, 265.3, 266.6, 267, 268, 268.3, DIG.1 [IMAGE AVAILABLE]

85. 4,287,562, Sep. 1, 1981, Real time adapter unit for use in a data processing system; Boyd E. Darden, et al., 395/559; 364/238.3, 238.6, 238.7, 239, 239.4, 240, 240.1, 242.4, 243, 243.3, 244, 244.3, 244.6, 244.7, 249, 249.2, 251, 251.1, 251.3, 252, 255.1, 255.2, 258, 259, 259.2, 262.4, 262.8, 270, 270.1, 280, 281.3, DIG.1; 395/557 [IMAGE AVAILABLE]

86. 4,286,319, Aug. 25, 1981, Expandable inter-**computer** communication system; Robert J. Membrino, et al., 395/200.01; 364/222.2, 228.3, 230, 230.4, 232.3, 239, 239.9, 240, 242.3, 242.5, DIG.1; 395/250 [IMAGE AVAILABLE]

87. 4,272,829, Jun. 9, 1981, Reconfigurable register and logic circuitry device for selective connection to external **buses**; Carson T. Schmidt, et al., 395/800; 327/403; 364/927.8, 932, 933, 933.3, 934, 935, 935.2, 935.3, 935.4, 935.45, 935.46, 936.1, 937.1, 940, 940.1, 940.2, 942.3, 942.4, 946.2, 946.6, 947, 947.1, 947.4, 948.1, 964, 964.2, DIG.2 [IMAGE AVAILABLE]

88. 4,270,167, May 26, 1981, Apparatus and method for cooperative and concurrent coprocessing of digital information; Robert J. Koehler, et al., 395/292; 364/228.3, 228.6, 229, 229.2, 230, 230.5, 232.3, 232.8, 240, 240.1, 240.5, 242.6, 242.92, 244, 244.3, 258, 258.1, 258.4, 262.4, 262.8, 263, 264, 264.6, 270, 271, 271.2, DIG.1 [IMAGE AVAILABLE]

89. 4,245,301, Jan. 13, 1981, Information processing system; Takashi Rokutanda, et al., 395/287; 364/228.3, 229, 229.1, 230, 230.4, 231.4, 232.9, 238, 238.3, 238.4, 240, 240.1, 240.2, 240.5, 240.8, 240.9, 241.2, 241.3, 241.9, 242.31, 259, 259.5, 264, 264.6, 265, 265.1, 265.3, 266.3, 273.4, DIG.1

[IMAGE AVAILABLE]

90. 4,234,926, Nov. 18, 1980, System & method for monitoring & diagnosing faults in environmentally **controlled** containers, such system and method being especially adapted for remote **computer controlled** monitoring of numerous transportable containers over existing on-site power wiring; Clifford G. Wallace, et al., 364/551.01, 131, 138, 185, 919, 919.5, 920, 921.8, 926, 927, 927.2, 927.4, 927.8, 927.82, 927.83, 927.92, 927.95, 927.99, 929.4, 930, 931, 931.4, 932.8, 935, 935.2, 935.3, 937, 939, 939.5, 940, 940.1, 940.2, 942, 943.9, 944.91, 947, 947.2, 949, 949.5, 952, 952.1, 959.1, 964, 964.1, 965, 965.5, 965.76, DIG.2 [IMAGE AVAILABLE]

91. 4,232,199, Nov. 4, 1980, Special services add-on for dial pulse activated telephone switching office; John T. Boatwright, et al., 379/197, 201, 205, 243, 246 [IMAGE AVAILABLE]

92. 4,216,532, Aug. 5, 1980, Self-correcting solid-state mass memory organized by words for a stored-program **control** system; Enzo Garetti, et al., 365/189.07, 200, 230.03, 238 [IMAGE AVAILABLE]

93. 4,131,941, Dec. 26, 1978, Linked microprogrammed plural processor system; Harvey L. Siegel, et al., 395/200.05; 364/228, 228.3, 229, 229.4, 230, 230.4, 242.4, 245, 245.1, 251, 251.1, 254.9, 258, 261.3, 261.5, 262.4, 262.8, DIG.1 [IMAGE AVAILABLE]

94. 4,096,566, Jun. 20, 1978, Modular signal processor having a hierarchical structure; Jean-Claude Borie, et al., 395/306; 364/222.2, 222.3, 230, 230.3, 230.4, 231.4, 231.6, 232.7, 238, 238.5, 240.1, 241.2, 241.3, 241.4, 241.5, 244, 244.6, 244.7, 251, 251.6, 252, 258, 258.1, 258.2, 259, 259.1, 259.7, 260.4, 260.9, 263, DIG.1 [IMAGE AVAILABLE]

```
=> D HIS

     (FILE 'USPAT' ENTERED AT 15:24:05 ON 07 MAY 1997)

                SET PAGE SCROLL
L1         31815 S BIDIRECTION## OR BI(2A)DIRECTION##
L2           509 S (FIRST(2A)L1) AND (SECOND(2A)L1)
L3           189 S L2 AND INTERFAC##
L4           189 S L2(P)INTERFACE#
L5           134 S L3 AND BUS
L6            20 S L5 AND PRINTER#
L7            20 S L6 AND CONTROL##
L8           130 S L5 AND (PRINT### OR DISPLAY### OR READ###)
L9           130 S L8 AND CONTROL####
L10           94 S L9 AND (PC OR COMPUTER)

=>  S L9 (NOT) L10
MISSING OPERATOR 'L9 (NOT'

=> S L9 NOT L10
L11          36 L9 NOT L10

=> D L11 1-36
```

1. 5,628,026, May 6, 1997, Multi-dimensional data transfer in a data processing system and method therefor; Natan Baron, et al., 395/821, 842 [IMAGE AVAILABLE]

2. 5,608,730, Mar. 4, 1997, Bi-directional communication system; Yoshio

Osakabe, et al., 370/471; 340/825.5; 348/13; 370/522; 395/288 [IMAGE AVAILABLE]

3. 5,598,413, Jan. 28, 1997, Four-wire, half-rate architecture with embedded differential delay compensation for extending range of basic rate ISDN communications; Michael S. Sansom, et al., 370/468, 516, 536 [IMAGE AVAILABLE]

4. 5,592,653, Jan. 7, 1997, **Interface** conversion device; Juan A. Guedan, et al., 395/500; 364/222.2, 239, 239.1, DIG.1; 370/465; 395/412, 484, 800 [IMAGE AVAILABLE]

5. 5,568,403, Oct. 22, 1996, Audio/video/data component system **bus**; Michael S. Deiss, et al., 364/514R; 370/468, 473 [IMAGE AVAILABLE]

6. 5,519,410, May 21, 1996, Virtual image **display** management system with head-up **display**; Joseph P. Smalanskas, et al., 345 /7; 340/980 [IMAGE AVAILABLE]

7. 5,448,562, Sep. 5, 1995, Bi-directional **bus** system and transmitting, receiving, and communication methods for same; Yoshio Osakabe, et al., 370/392, 474 [IMAGE AVAILABLE]

8. 5,425,027, Jun. 13, 1995, Wide area fiber and TV cable fast packet cell network; Paul Baran, 370/395; 340/825.08; 348/11; 370/432, 449, 480, 906 [IMAGE AVAILABLE]

9. RE 34,946, May 23, 1995, Method and apparatus for adjusting a shear bar relative to a cutter head; Marvin G. Weaver, et al., 241/30, 37, 101.71, 241; 340/684, 686 [IMAGE AVAILABLE]

10. 5,402,419, Mar. 28, 1995, Transmitting method, receiving method, and communication method for bi-directional **bus** system, and bi-directional **bus** system; Yoshio Osakabe, et al., 370/3 92; 340/825.07, 825.52; 348/8; 370/395, 522 [IMAGE AVAILABLE]

11. 5,377,325, Dec. 27, 1994, Bidirectional wait **control** between host module and slave module; Wan-Kan Chan, 395/849, 551 [IMAGE AVAILABLE]

12. 5,252,902, Oct. 12, 1993, Servo **control** system; Shinichiro Uehara, et al., 318/599, 600; 388/811, 815 [IMAGE AVAILABLE]

13. 5,157,775, Oct. 20, 1992, Dual port, dual speed image memory access arrangement; Kurt M. Sanger, 395/405; 364/237.2, 238, 238.6, 238.7, 239, 239.1, 239.2, 239.9, 240, 240.2, 243, 244, 244.8, 246.91, 247, 247.8, 254, 259, 259.5, 259.9, 260, 260.1, 263.1, 920.7, 927.2, 927.3, 927.92, 927.97, 933, 933.3, 937.01, 942, 964, 964.2, 964.31, 965, 965.9, 977.5, DIG.1, DIG.2; 365/230.05 [IMAGE AVAILABLE]

14. 5,093,784, Mar. 3, 1992, Data processor with efficient transfer between subroutines and main program; Syuichi Hanatani, 395/569; 364/228.2, 228.8, 232.1, 232.3, 247, 255.1, 258.1, 261.5, 262.8, DIG.1; 395/589 [IMAGE AVAILABLE]

15. 5,089,953, Feb. 18, 1992, **Control** and arbitration unit; Frank J. Ludicky, 395/293; 364/228, 228.6, 229, 229.5, 230, 230.6, 231.3, 231.5, 231.7, 239, 239.7, 239.8, 240, 240.5, 240.8, 240.9, 242.6, 242.91, 242.92, 243, 243.5, 260, 260.1, 260.2, DIG.1; 395/800 [IMAGE AVAILABLE]

16. RE 33,629, Jul. 2, 1991, Numeric data processor; John F. Palmer, et al., 364/748, 258, 737, 745 [IMAGE AVAILABLE]

17. 4,945,536, Jul. 31, 1990, Method and apparatus for testing digital systems; Marius Hancu, 371/22.3, 22.1 [IMAGE AVAILABLE]

18. 4,939,718, Jul. 3, 1990, Routing method and packet switching networks having a distance indicator for routing; Michel Servel, et al., 370/410 [IMAGE AVAILABLE]

19. 4,914,619, Apr. 3, 1990, Apparatus and method for interconnecting an application of a transparent services access facility to remote source; John F. Harris, et al., 395/200.09; 364/228.2, 232.1, 926.1, 926.93, 927.92, 927.96, 929, 930, 931, 931.4, 931.43, 933.9, 935, 935.2, 935.3, 935.4, 940, 940.61, 940.64, 940.81, 941, 943.9, 946.2, 947, 950.1, 964.1, 976, 978.1, DIG.2 [IMAGE AVAILABLE]

20. 4,839,830, Jun. 13, 1989, Apparatus and method for the processing of operating data of an electric motor; Walter Amey, et al., 364/551.01, 508 [IMAGE AVAILABLE]

21. 4,799,625, Jan. 24, 1989, Method and apparatus for adjusting a shear bar relative to a cutter head; Marvin G. Weaver, Jr., et al., 241/30, 37, 101.71, 241; 340/684, 686 [IMAGE AVAILABLE]

22. 4,791,341, Dec. 13, 1988, Speed reducing **control** system for a polyphase electric motor; Herbert J. Brown, et al., 318/809, 812 [IMAGE AVAILABLE]

23. 4,785,473, Nov. 15, 1988, Interactive audio telecommunications message storage, forwarding and retrieval system; Randall R. Pfeiffer, et al., 379/89, 84 [IMAGE AVAILABLE]

24. 4,718,057, Jan. 5, 1988, Streamlined digital signal processor; P. Venkitakrishnan, et al., 370/229, 458, 524 [IMAGE AVAILABLE]

25. 4,635,255, Jan. 6, 1987, Digital subscriber **controller**; Alan T. Clark, et al., 370/524 [IMAGE AVAILABLE]

26. 4,509,144, Apr. 2, 1985, Programmable bidirectional shifter; John Palmer, et al., 364/715.08, 926.9, 926.91, 931.4, 931.48, 931.49, 942.3, 942.4, 948.3, 948.32, DIG.2 [IMAGE AVAILABLE]

27. 4,472,798, Sep. 18, 1984, Telecommunication path substitution arrangement; Edward H. Hafer, 370/248, 370, 376 [IMAGE AVAILABLE]

28. 4,470,113, Sep. 4, 1984, Information processing unit; Toshio Oura, 395/306; 364/221, 221.6, 228.4, 228.6, 229, 229.2, 230, 230.4, 232.7, 232.8, 232.9, 238.3, 240, 240.1, 240.2, 240.4, 240.5, 241.9, 242.1, 260, 260.1, 275.7, 275.9, 284, DIG.1 [IMAGE AVAILABLE]

29. 4,461,985, Jul. 24, 1984, Speed reducing **control** system for a polyphase electric motor; Thomas D. Stitt, 318/727, 772 [IMAGE AVAILABLE]

30. 4,413,337, Nov. 1, 1983, Time division switching system for circuit mode and packet mode lines; Jean-Louis Dauphin, et al., 370/352, 366 [IMAGE AVAILABLE]

31. 4,360,891, Nov. 23, 1982, Address and data **interface** unit; Michael H.

Branigin, et al., 395/384; 364/927.8, 933, 933.7, 935, 935.2, 935.3, 935.45, 935.46, 937.1, 937.2, 937.8, 940, 942, 942.8, 943.9, 944.4, 945.6, 947, 947.1, 947.6, 951.1, 951.3, 965, 965.5, 968, DIG.2 [IMAGE AVAILABLE]

32. 4,338,675, Jul. 6, 1982, Numeric data processor; John F. Palmer, et al., 364/748, 224, 230, 230.4, 232.8, 240, 244, 244.3, 247, 247.8, 258, 258.1, 258.2, 258.3, 258.4, 259, 259.5, 259.7, 260.4, 260.9, 263, 263.1, 264, 264.2, 265, 265.4, 266.4, 271, 271.2, 715.08, 737, 745, DIG.1 [IMAGE AVAILABLE]

33. 4,317,171, Feb. 23, 1982, LSI Microprocessor having an error processing circuit; Hideo Maejima, et al., 395/591; 364/228, 228.3, 231.8, 232.8, 241.2, 241.5, 242.3, 242.31, 244, 244.6, 246.6, 246.7, 260.4, 260.8, 265, 266, 266.3, 267, 267.4, 267.6, 271, 271.4, DIG.1; 395/183.18 [IMAGE AVAILABLE]

34. 4,307,645, Dec. 29, 1981, Electronic apparatus for teaching and **reading** music; Francesco Rauchi, 84/678, 462, 470R, 649, 653; 984/302, DIG.1 [IMAGE AVAILABLE]

35. 4,296,469, Oct. 20, 1981, Execution unit for data processor using segmented **bus** structure; Thomas G. Gunter, et al., 395/308; 364/232.8, 234, 234.4, 238, 239, 239.4, 240, 240.1, 240.2, 240.7, 244, 244.3, 244.7, 244.8, 249, 249.1, 251, 251.1, 251.3, 252, 252.3, 252.6, 252.7, 254, 254.1, 258, 258.1, 258.2, 258.3, 262.4, 262.5, 263, DIG.1 [IMAGE AVAILABLE]

36. 4,093,982, Jun. 6, 1978, Microprocessor system; Dale Arthur Heuer, et al., 395/598; 364/228.1, 228.3, 232.8, 243, 244, 244.4, 244.6, 245, 245.3, 258, 258.1, 259, 262.4, 262.8, 270, 271.6, DIG.1; 395/200.06 [IMAGE AVAILABLE]

=> D HIS

(FILE 'USPAT' ENTERED AT 15:24:05 ON 07 MAY 1997)

SET PAGE SCROLL

L1 31815 S BIDIRECTION## OR BI(2A)DIRECTION##
L2 509 S (FIRST(2A)L1) AND (SECOND(2A)L1)
L3 189 S L2 AND INTERFAC##
L4 189 S L2(P)INTERFACE#
L5 134 S L3 AND BUS
L6 20 S L5 AND PRINTER#
L7 20 S L6 AND CONTROL##
L8 130 S L5 AND (PRINT### OR DISPLAY### OR READ###)
L9 130 S L8 AND CONTROL####
L10 94 S L9 AND (PC OR COMPUTER)
L11 36 S L9 NOT L10

=> S L10 AND (COLOR OR COLOUR)
204031 COLOR
62138 COLORS
214665 COLOR
(COLOR OR COLORS)
24966 COLOUR
4735 COLOURS
26316 COLOUR
(COLOUR OR COLOURS)
L12 9 L10 AND (COLOR OR COLOUR)

=> D L12 1-9

1. 5,541,640, Jul. 30, 1996, Videophone for simultaneous audio and video

communication via a standard telephone line; Craig R. Larson, 348/19; 379/96 [IMAGE AVAILABLE]

2. 5,481,542, Jan. 2, 1996, Interactive information services **control** system; Gary L. Logston, et al., 348/7, 13; 370/442, 461, 473, 474 [IMAGE AVAILABLE]

3. 5,420,696, May 30, 1995, Image data transfer architecture and method for an electronic reprographic machine; Donald L. Wegeng, et al., 358/468; 345/190; 358/406; 395/526 [IMAGE AVAILABLE]

4. 5,379,052, Jan. 3, 1995, VGA and EGA video **controller** apparatus using shared common video memory; Jeffrey A. Walck, et al., 345/185, 132 [IMAGE AVAILABLE]

5. 5,144,314, Sep. 1, 1992, Programmable object identification transponder system; Eric Malmberg, et al., 342/44, 51 [IMAGE AVAILABLE]

6. 5,128,996, Jul. 7, 1992, Multichannel data encryption device; Michael J. Rosenow, et al., 380/21; 235/380; 380/25, 49 [IMAGE AVAILABLE]

7. 5,056,041, Oct. 8, 1991, Data processing apparatus with improved bit masking capability; Karl M. Guttag, et al., 395/521; 345/191; 395/513 [IMAGE AVAILABLE]

8. 4,908,823, Mar. 13, 1990, Hybrid communications link adapter incorporating input/output and data communications technology; Randolph B. Haagens, et al., 370/464; 340/825.03, 825.2, 825.5; 359/158, 163; 370/466; 375/222 [IMAGE AVAILABLE]

9. 4,485,402, Nov. 27, 1984, Video image processing system; Anthony D. Searby, 348/715 [IMAGE AVAILABLE]

=>